32 pages

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Final Report

"Development of Optimized Detector/Spectrophotometer Technology for Low Background Space Astronomy Missions"

11/1/82 - 4/30/85

Contract NASW-3702 UCSD 488870/26360

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Scientific Goals and Achievements of the Research

This program was directed towards the better understanding of some of the important factors in the performance of infrared detector arrays at low background conditions as appropriate for space astronomy. The arrays were manufactured by Aerojet Electrosystems Corporation, Azusa. Two arrays, both bismuth doped silicon, were investigated: an AMCID 32x32 "Engineering mosiac Si:Bi accumulation mode charge injection device detector array" which was purchased with funds from this contract, and a MOS-FET switched array of 16x32 pixels which was made available to this program by another concurrent research effort sponsored by UC/MICRO and Aerojet Electrosystems. (UC/MICRO is a collaborative program with funding from both the University of California and industry - Microelectronics Innovation and Computer Research Opportunities.)

In order to test the arrays in a suitable low temperature environment a cryogenic "spot-scanner" was designed and constructed. The scanner uses a modified model 982-68 special 68 pin infrared test dewar from Hansen and Associates to provide cooling (this is based on the Air Products Heli-trans helium cooling system). There are three independently controlled cold stations: the detector (variable from 2.7 to 50K), the ambient background optics (20 to 150K), and the blackbody source (50 to 300K). Temperature control is achieved through a balance of helium flow rate, vent pressure and heaters. The temperature is monitored with silicon diodes, and can be held to a stability of 0.1K. Optics are used to reimage a spot of radiation from the blackbody onto the array. The spot can be scanned in X and Y over the array and moved in Z to achieve best focus. An internal filter tray and chopper are also available.

The schematic mechanical diagram of the scanner and photographs of the assembled system and details of several subsystems are shown Appendix A.

The 32x32 AMCID array which was ordered in December of 82 was not delivered until March of 84 due to manufacturing difficulties. The active area achieved was 10x16 pixels. Data on this detector is presented in Appendix B, together with schematics of the readout and control circuitry constructed. The noise level achieved in the readout electronics for the AMCID was 45 electrons. This array was not put into the spot scanner for testing due to 2 developments - the scanner acquired a vacuum leak which

required extensive rework of the liquid nitrogen shield, delaying its use until the end of 1984, and by this time the MOS-FET multiplexed array was close to delivery and since it was reported to be a much superior detector, efforts were redirected towards this device.

The 16x32 MOS-FET multiplexed array was delivered in 1985. The readout and control circuitry were partially designed and constructed with funds from this contract. Following the close of the contract work on the array was continued using other funds since the array shows considerable potential for astronomical use. The technical details of the array and our readout electronics are presented in Appendix C.

Publications

"A Grating Array Spectrophotometer for the 10 Micron Wavelength Region" B. Jones, R.G. Hier, S.E. Nelson, R.C. Puetter, and G.W. Schmidt. 1983 Proc. SPIE 445, 108.

"A low noise Infrared Spot Scanner for Testing Detector Arrays" R.C. Puetter, P. Brissenden, J. Casler, R.G. Hier, and B. Jones 1983, Proc. SPIE 445, 162.

"A Charge Sensitive Readout Technique for Infrared Photoconductors" G.W. Schmidt, R.G. Hier, S.E. Nelson, and R.C. Puetter. 1985, Advances in Electronics & Electron Physics, Vol 64A, 251.

Appendix A

Mechanical Details and Photographs of the Spot Scanner

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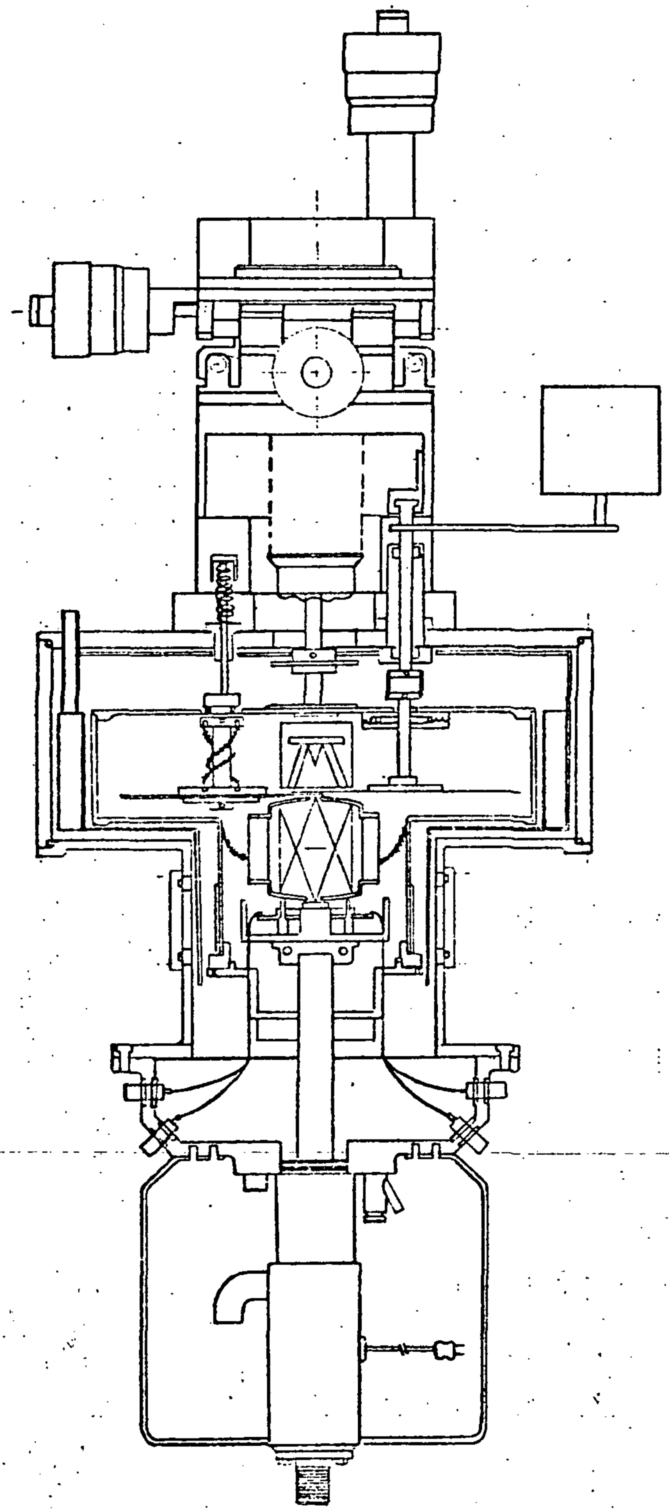

Figure 1. Mechanical diagram of the IR spot scanner showing x-y-z manipulator (top) cryo-optics section (middle), and detector/electronics/cooling system (bottom).

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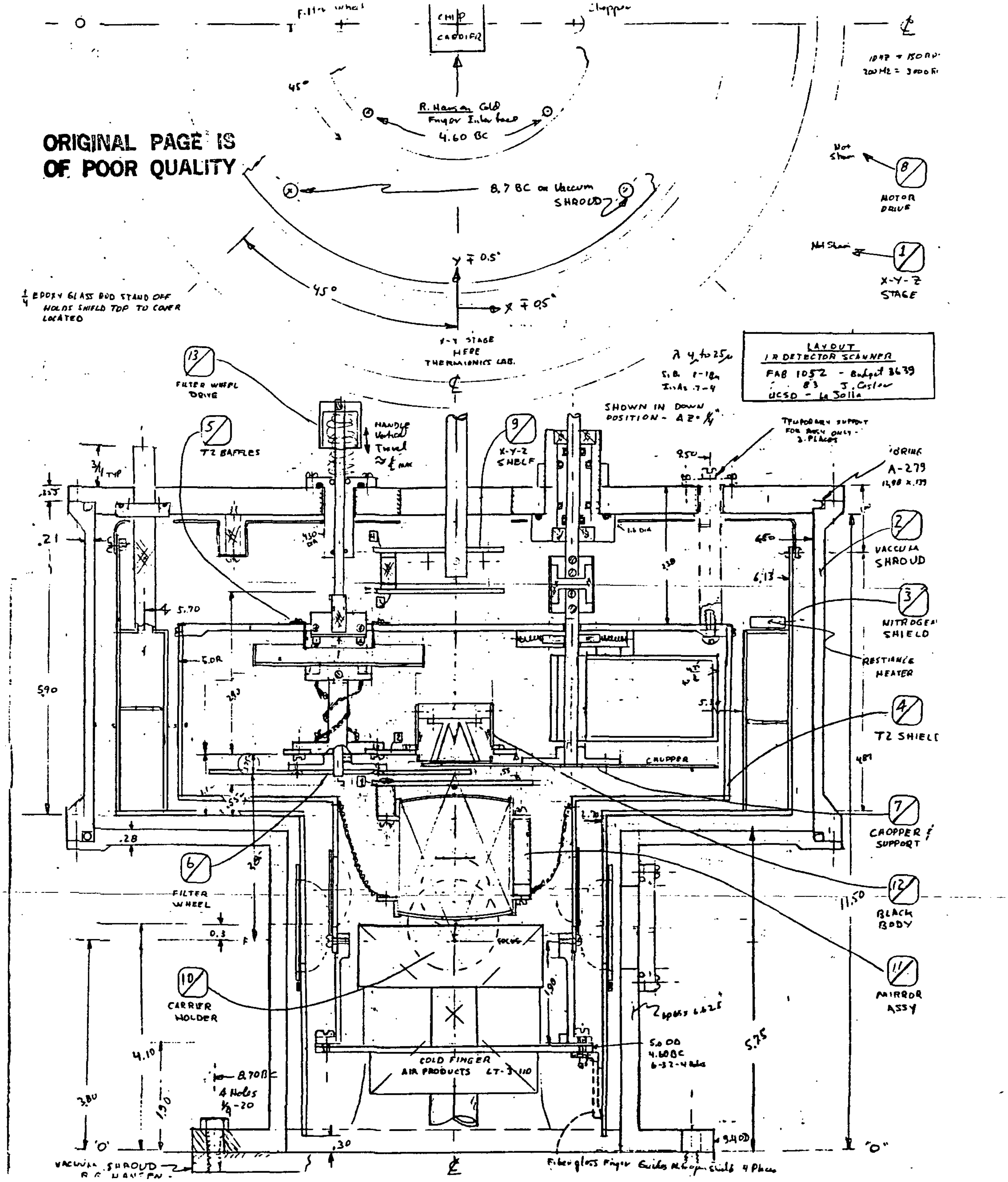

Figure 2. Details of mechanical layout of spot-scanner.

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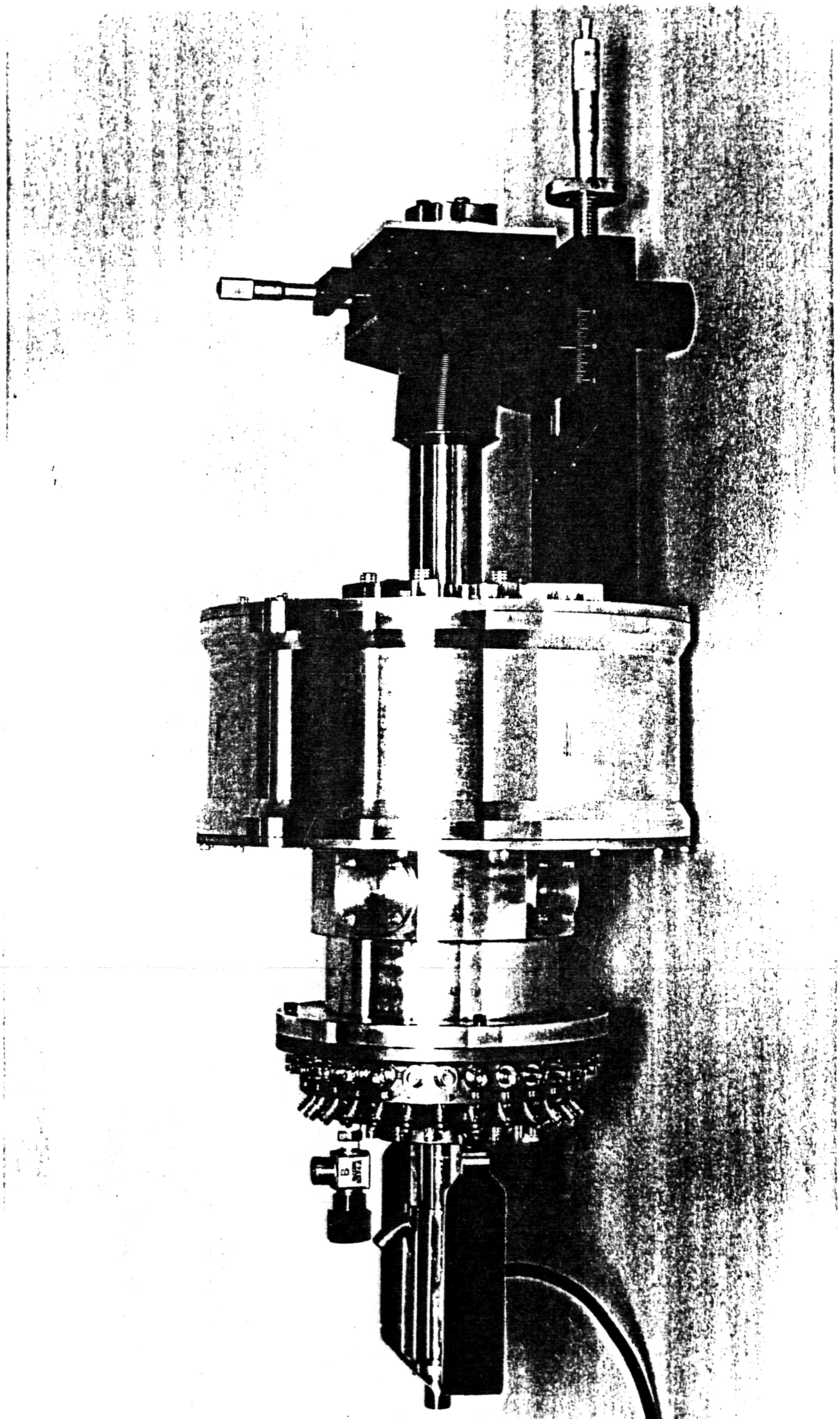

Figure 3. Assembled spot-scanner.

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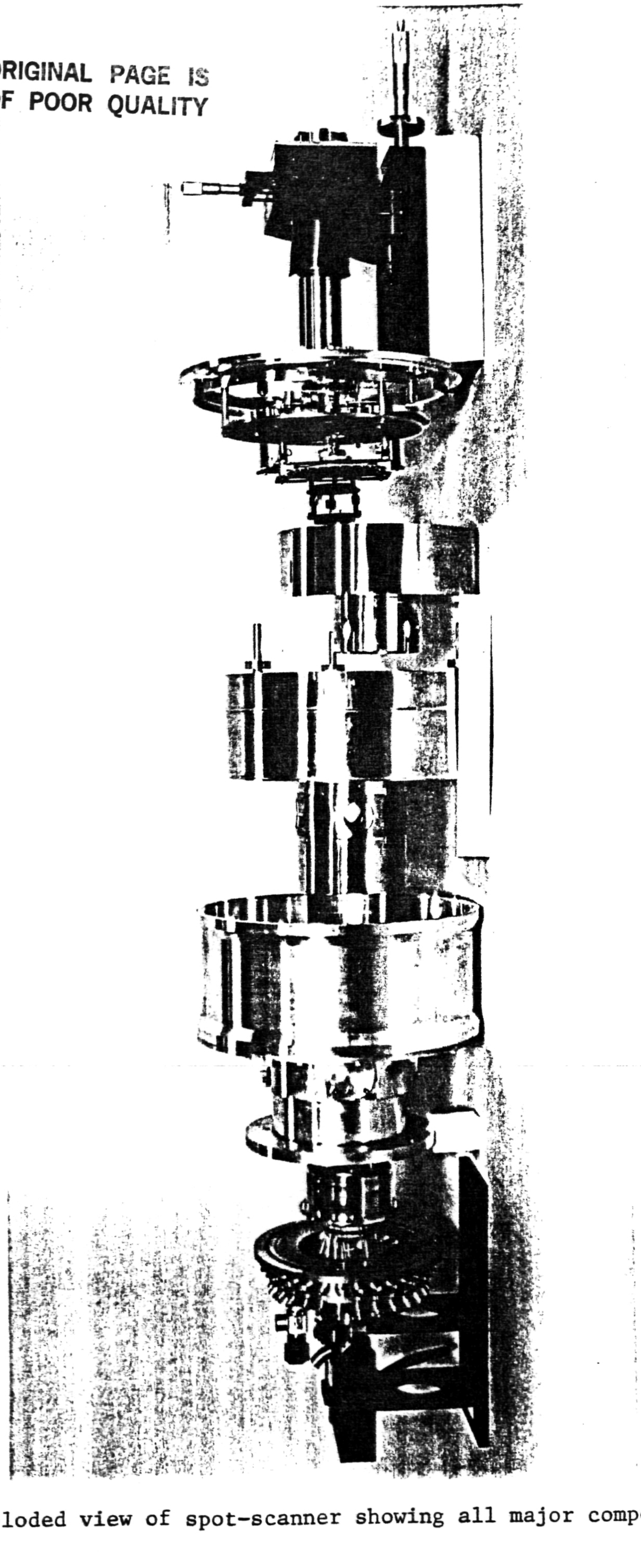

Figure 4. Exploded view of spot-scanner showing all major components.

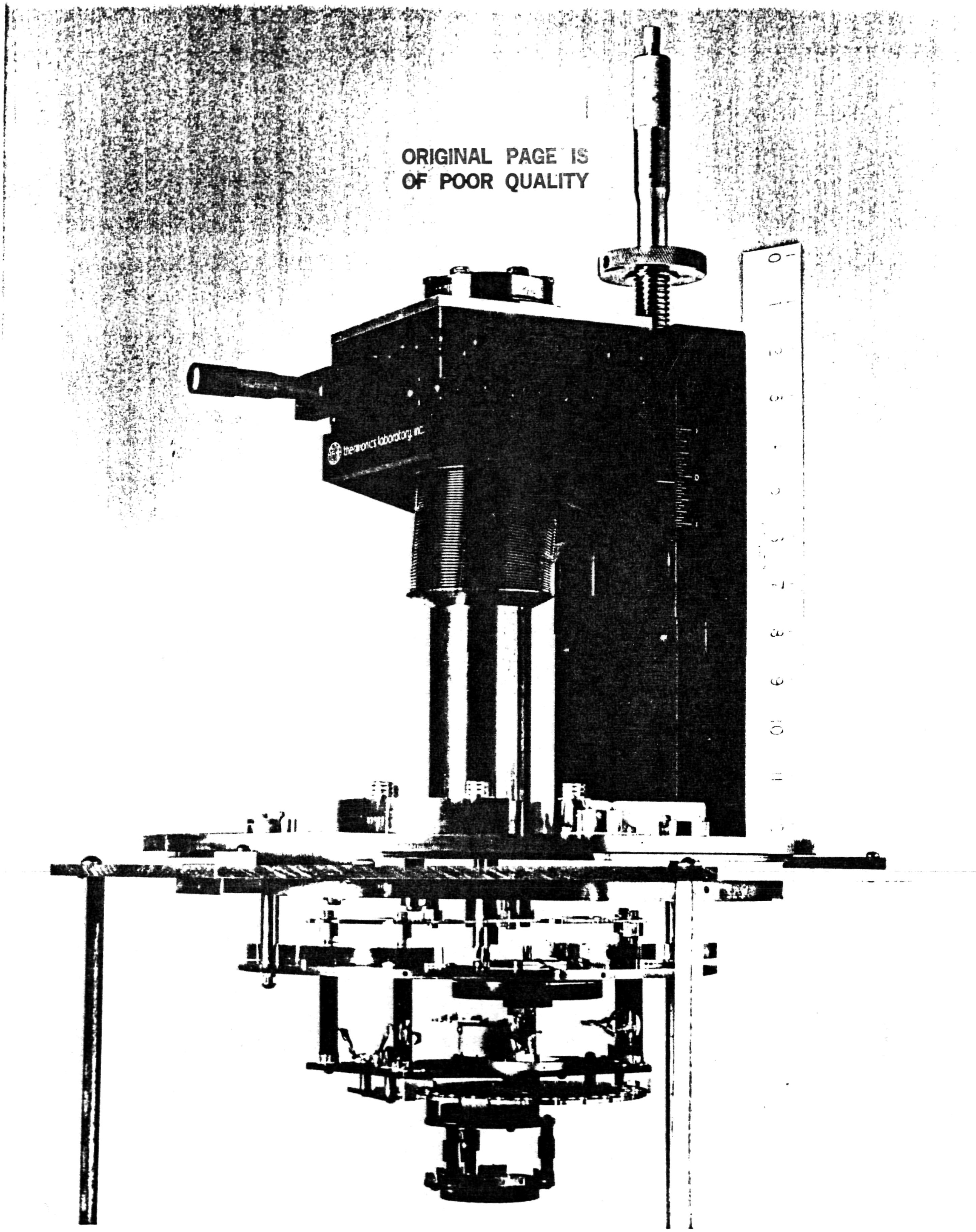

Figure 5. View of optics assembly and x-y stage.

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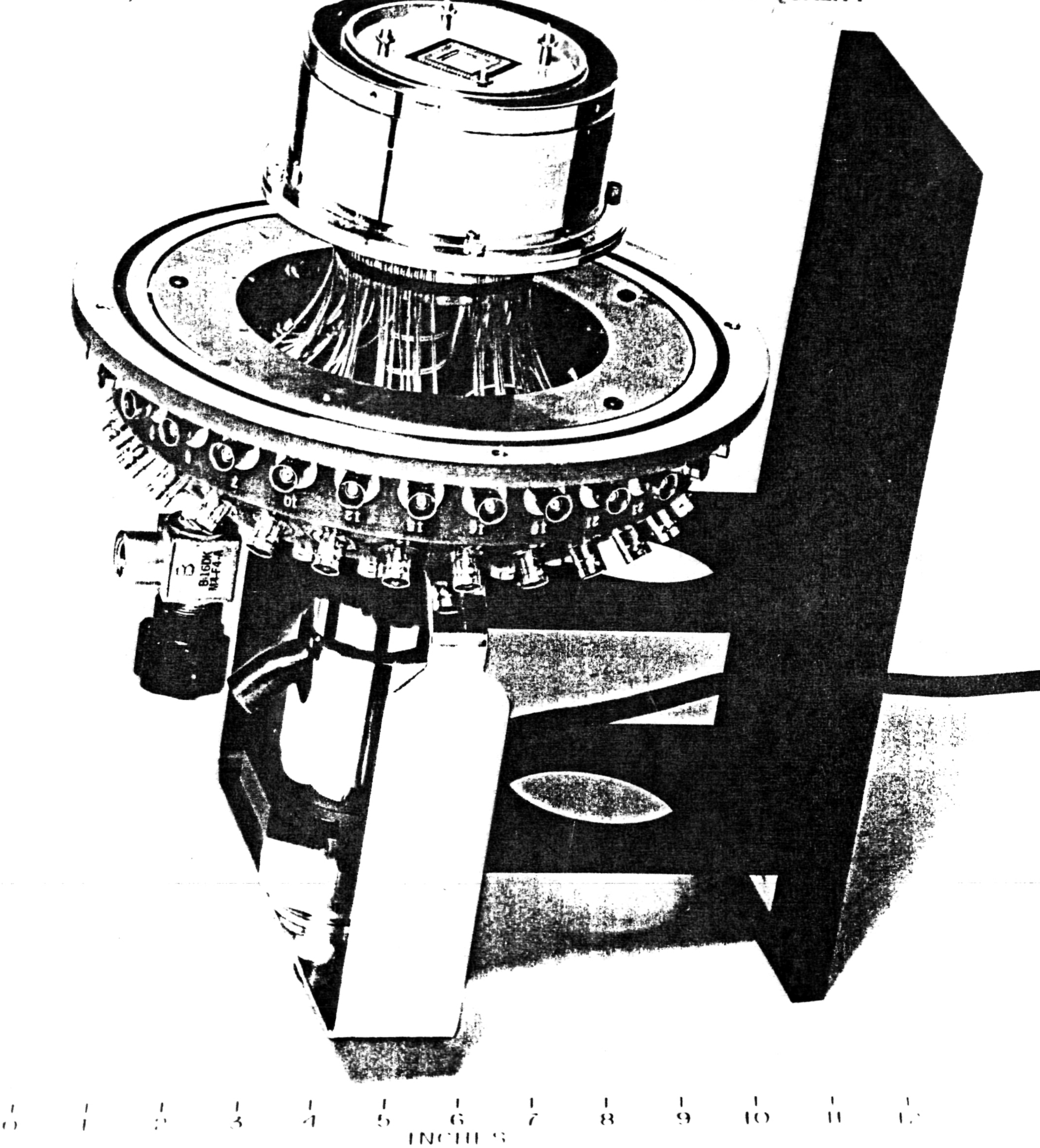

Figure 6. Detailed view of detector, electronics and cooling section.

Appendix B

The 32x32 (16x10 active) AMCID Array

AMCID AND EXTRINSIC SILICON DETECTORS

Purchase Order E73120-3639

Prepared for

University of California, San Diego
Center for Astrophysics and Space Sciences
La Jolla, California 92093

Report 6793 February 1984

AEROJET ELECTROSYSTEMS COMPANY
A DIVISION OF AEROJET GENERAL
1100 WEST HOLLYVALE STREET, AZUSA, CALIFORNIA 91702

1 INTRODUCTION

A 32x32-element, engineering mosaic array of bismuth-doped silicon, accumulation-mode charge-injection device (AMCID) detectors was designed, fabricated, evaluated, and delivered to the Center for Astrophysics and Space Sciences at the University of California at San Diego under Purchase Order E73120-3639. Also provided was a linear array of 12 operational Si:Bi photoconductors calibrated for use as background monitors.

The mosaic array included a multiplexed, fully operational, 10x16-element section with cryogenic on-focal-plane electronics, suitable for operation at 10 K and capable of performing pixel scanning and output-signal buffering. It was packaged in a form suitable for operation in a cryostat that has a 68-pin leadless carrier as the mount. The device was characterized using infrared signals generated by a light-emitting diode (LED).

The 12-element linear array was provided in a 22-pin flatpack package having a common bias line and individual 100-pF capacitors for operation with a transcapacitance amplifier. The photoconductors were calibrated with a 500 K blackbody source, spike-filtered at a wavelength of 15 micrometers.

2 ARRAY DESCRIPTIONS

2.1 AMCID UNIT CELL

An AMCID-type device is a metal-oxide-semiconductor (MOS) capacitor whose operation in an infrared detection system depends on photoconduction in the semiconductor layer. A unit detector cell of the type delivered is shown in Figure 1, where R_G is gate load resistance, C_G stray gate capacitance, and V_{ss} source supply voltage. It operates as follows: Incoming photons (ϕ) pass through the transparent electrode and are absorbed in the Si:Bi layer. They liberate electrons that migrate toward the silicon dioxide dielectric because of the potential provided by V_{store}. Reversing bias, by switching to V_{read}, sweeps these charges out to the transparent electrode, where they are read out through the source follower.

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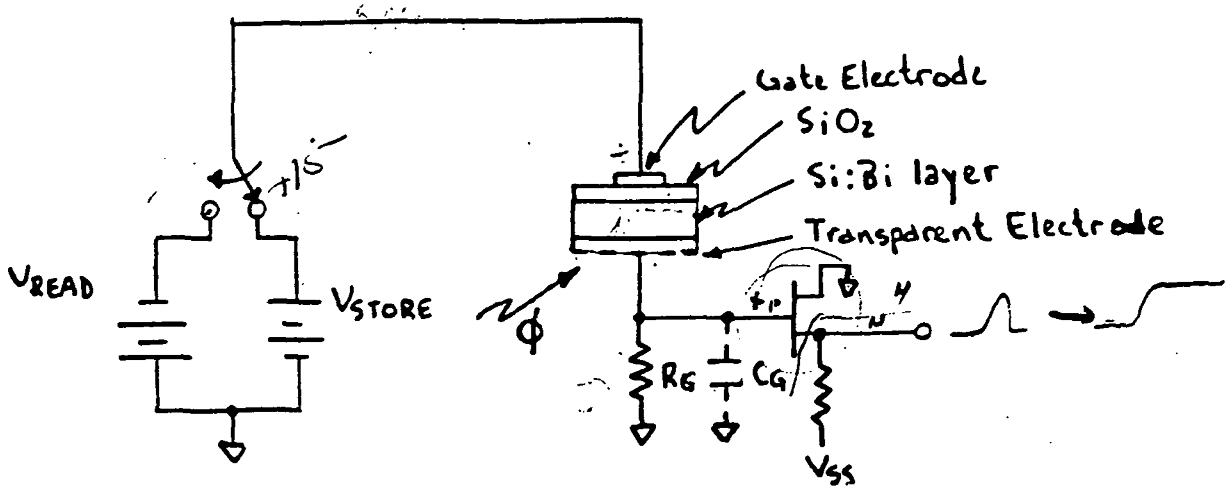


FIGURE 1 UNIT CELL

2.2 AMCID MOSAIC

Unit cells can be configured together to form an MxN mosaic as shown in Figure 2, where the squares represent gate electrodes. The individual gates are joined together to form columns perpendicular to the transparent-electrode strips that make up the rows. When fabricated, the individual gate pads are separated from each other; columns are formed by "stitch bonding" them together.

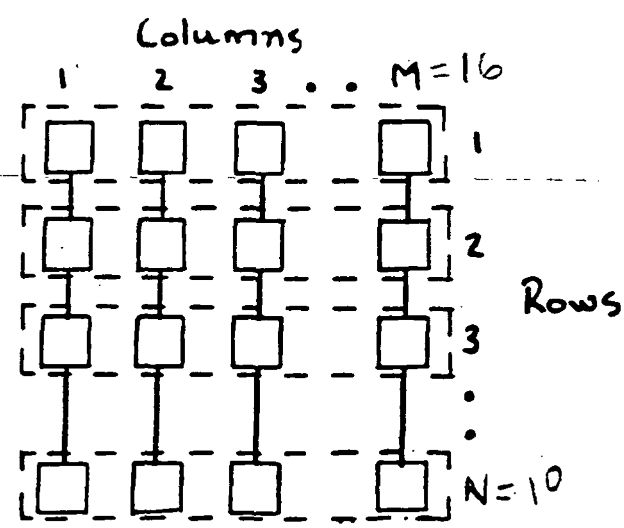


FIGURE 2 MOSAIC-ARRAY GEOMETRY

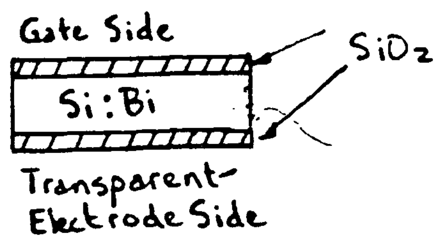
Operation of the mosaic is the same as described for the unit cell. By switching bias from V_{store} to V_{read}, from one column to the next, photogenerated charge under each gate in the column will be swept out to the transparent-electrode row lying below it. This charge will be read out by the row "source follower", making possible a matrix scan of the incoming infrared radiation.

2.3 GEOMETRY AND FABRICATION OF 32x32-ELEMENT AMCID

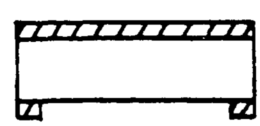
Figure 3 indicates the 32x32-AMCID gate size and guard dimensions. The guard is included so that pixels can be isolated electrically.

The steps in AMCID fabrication are as described below.

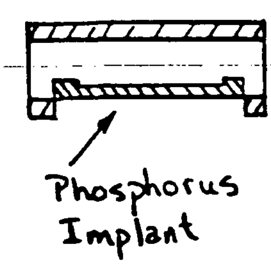
a. An oxide layer approximately 4000 angstroms thick is thermally grown on each side of a polished Si:Bi wafer.



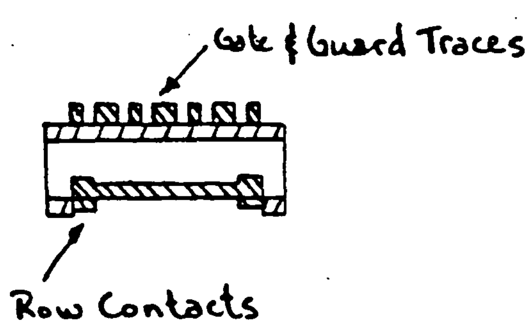
b. The wafer is masked and etched, selectively removing oxide on the transparent-electrode side.



c. The wafer is masked and transparent electrodes are implanted with phosphorus in two steps. One implant defines the contact region and is nontransparent; the other defines the row strips and is transparent.



d. The wafer is aluminized, masked, and etched to define (1) gate-side pads and guard rings, and (2) transparent-electrode contacts. The wafer is then sintered, probed, and diced.



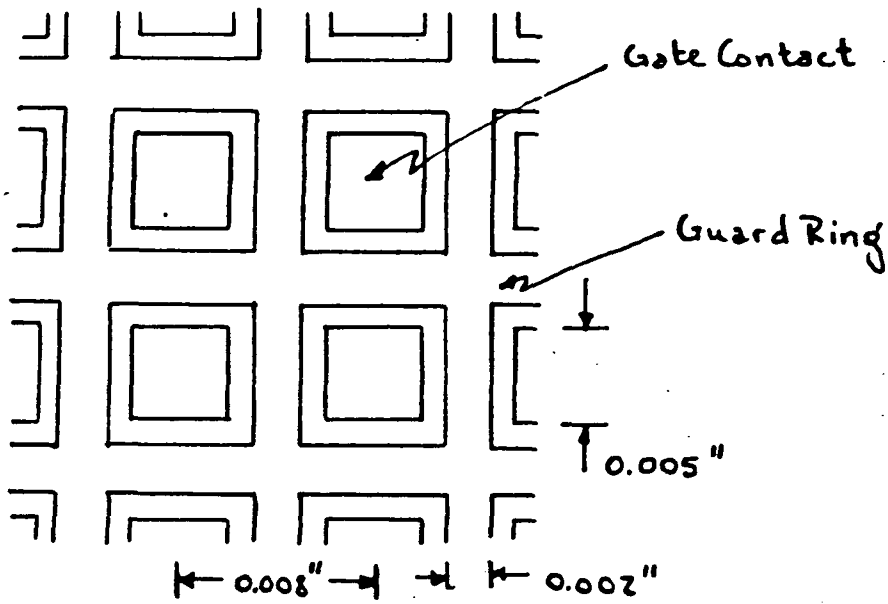


FIGURE 3 GATE GEOMETRY

2.4 SUBASSEMBLY ELECTRONICS

Noise and impedance-matching factors dictated that subassembly electronics be mounted near the detector and hence operate cryogenically. A complementary MOS (CMOS) 4- to 16-line demultiplexer (Type 54C154) was selected to provide bias switching. Provisions for wide variation in supply voltage (15 volts differential) at 10 K permit optimization of detector bias. Figure 4 shows the bias-switching scheme using the 54C154 device. Ten Type 3N164 MOSFETs were selected to serve as row-readout buffers. Minisystems, Inc. MSR3 devices were incorporated as load resistors; their resistance is approximately 30 megohms at 10 K. Carrier substrates of gold/titanium on 0.025-in. alumina were used to mount them in the focal plane package.

2.5 FOCAL PLANE PACKAGE

The package was sized for operation in a 68-pin leadless carrier as requested. Two Isotronics, Inc. flatpacks (IP-1088-1 and IP-1057-1) were machined and soldered together yielding a package height of 0.23 in. Prior to soldering, square holes were cut in both flatpacks to provide a mounting frame for the AMCID. The leads of the smaller flatpack were fed through the larger to serve as transparent-electrode connections for the MOSFETs. Biggs Company A+B Fast Epoxy Paste was introduced around the leads, isolating them from the larger case.

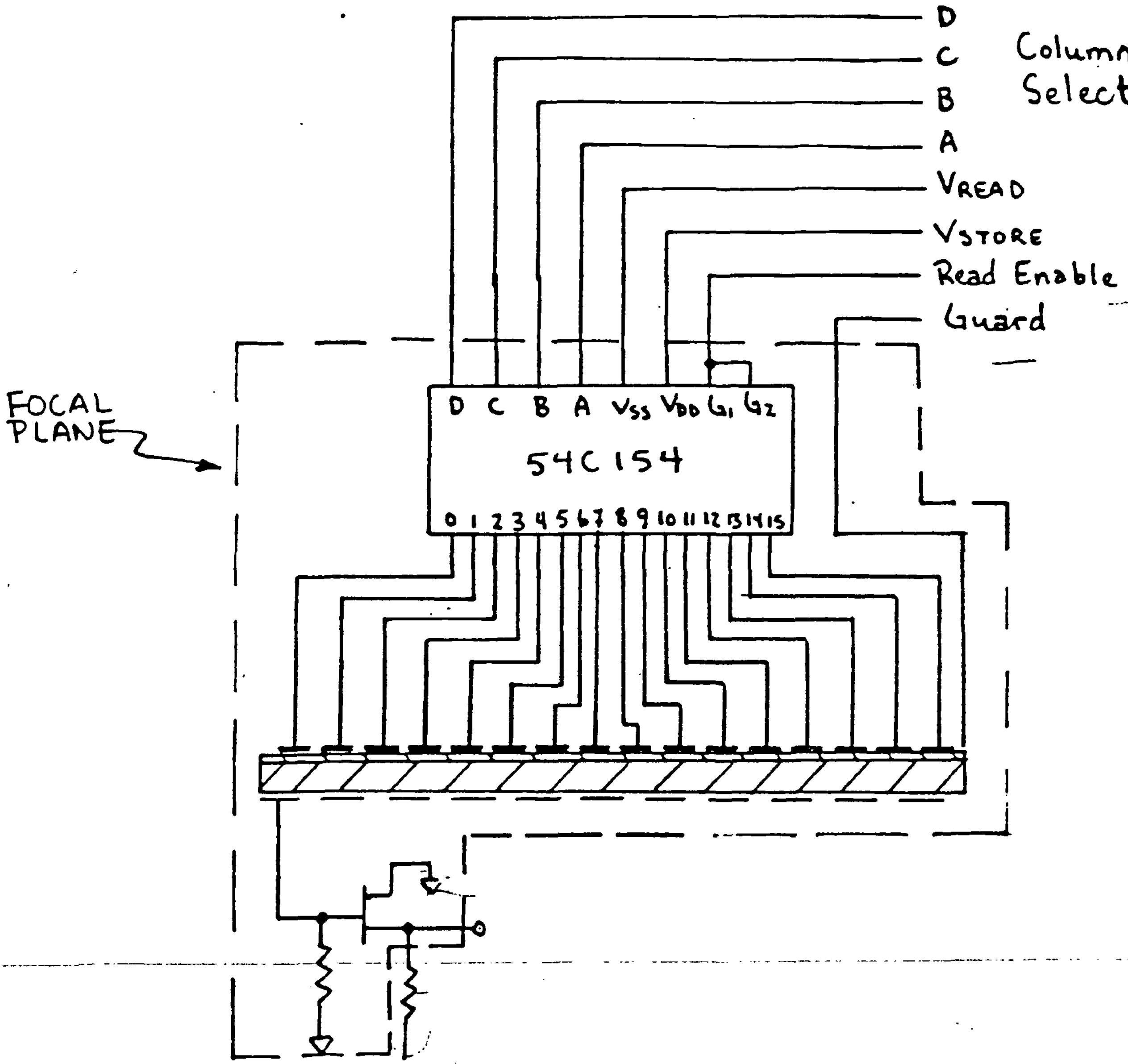


FIGURE 4 DEMULTIPLEXER-TO-AMCID INTERCONNECT

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Subassembly electronic substrates with components were mounted and wired in the larger case as shown in Figure 5. A ring of polyimide having copper traces plated with gold on 0.050-in. centers was provided for operation in the leadless carrier package.

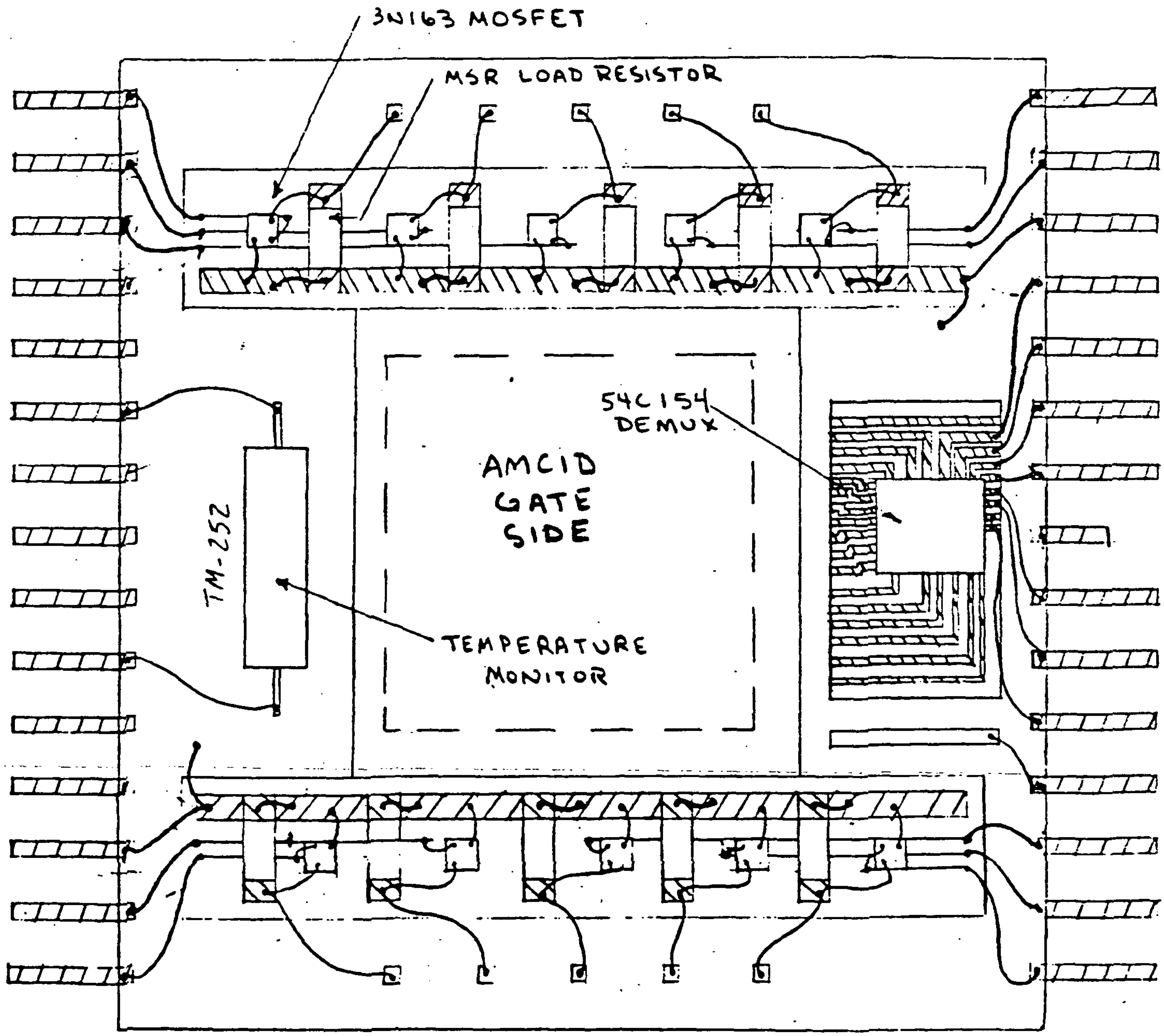

FIGURE 5 AMCID PACKAGE, COMPONENT SIDE

After final evaluation, the package was mounted on the ring; the leads were bent to meet the tracks below and were soldered. The pin-out locations are identified in a top view of the package presented in Figure 6 (where V_{SS} = multiplexer negative supply voltage; V_{DD} = positive supply voltage; A,B,C,D = column-select lines; S = source-follower source terminal; D = source-follower drain terminal; G = source-follower gain terminal; and TM = temperature monitor). For temperature monitoring, a 5.6-kilohm Allen-Bradley carbon resistor was epoxied in the package and was wired out; a TM calibration curve is presented in Figure 7.

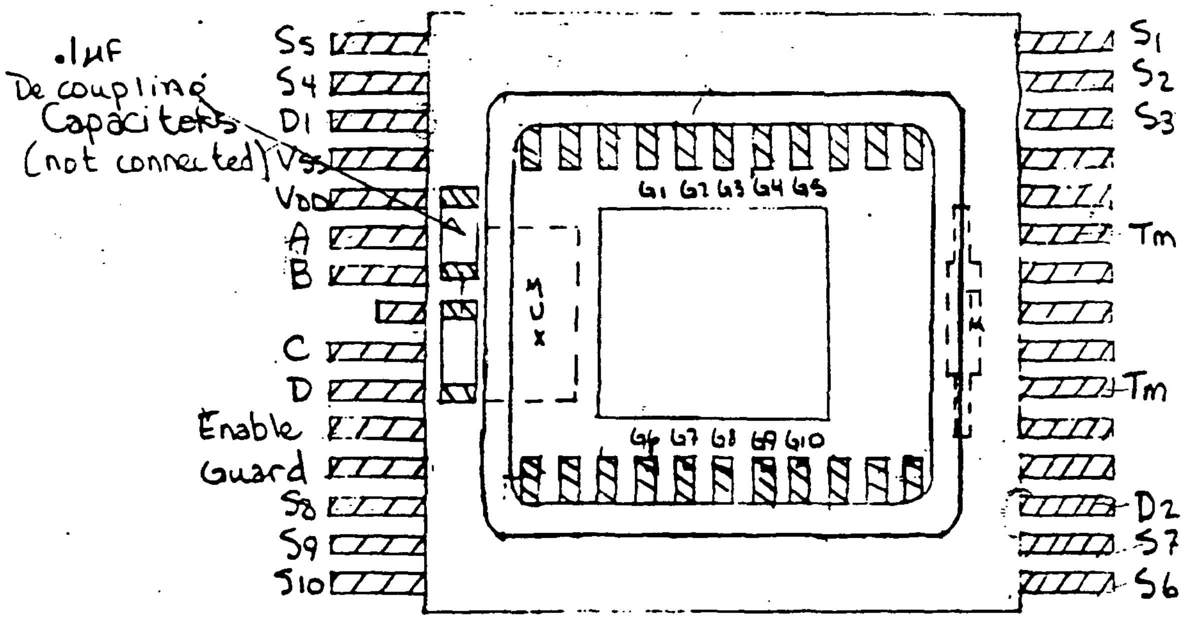

FIGURE 6 AMCID PACKAGE, TOP VIEW

2.6 LINEAR PHOTOCONDUCTOR ARRAY

Fifteen photoconductive detectors were constructed from a bar of Si:Bi 0.015 in. deep by 0.034 in. wide by 0.120 in. long, with a layer of gold on the back surface to provide a common bias contact. The top surface has two gold strips extending 0.007 in. within each outside edge for the entire length of the bar, leaving an exposed area of 0.020 x 0.120 in. The bar was mounted on a sapphire substrate and then in an Isotronics flatpack with silver epoxy. Individual detectors were delineated by making a 0.0015-in.-wide cut

4 EVALUATION OF AMCID DETECTOR ARRAY

4.1 CHARACTERIZATION OF ROW PREAMPLIFIERS

Before the AMCID detector array was installed in the focal plane package, each row-MOSFET gate load resistor was accessed and measured at 10 K using a voltage source and a Keithley 602 electrometer. Current was measured in both directions for each resistor, and resistance was calculated from the voltage divided by the average current. With the gate loads characterized, the AMCID was installed, the rows were connected to the MOSFET gates, and each load resistor was driven by a sinusoidal source of known amplitude. The MOSFET voltage gain and 3-dB rolloff frequency were measured with a Hewlett-Packard HP3581A wave analyzer as shown in Figure 14.

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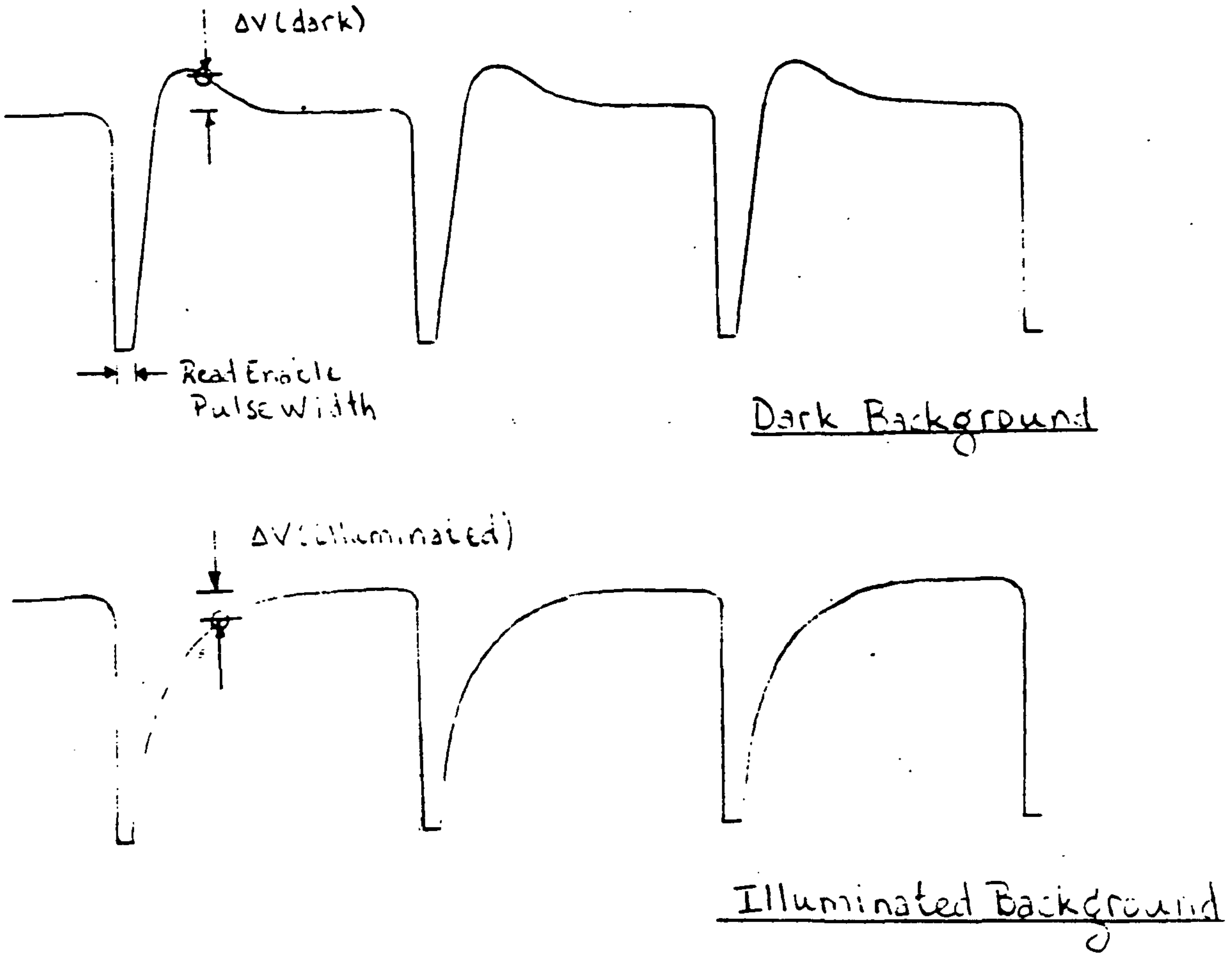

FIGURE 13 TYPICAL MOSFET OUTPUT BEFORE S/H

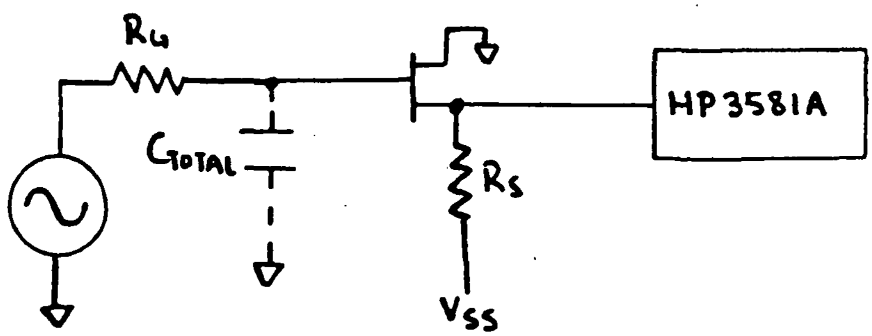

FIGURE 14 MOSFET CHARACTERIZATION TEST

The total input capacitance, C_{total} (AMCID stray capacitance shunted with MOSFET stray capacitance), was calculated from

$$C_{total} = \frac{1}{2\pi\ f\ R_G}$$

where the source frequency (f) equals the 3-dB rolloff frequency. Table 1 lists the preamplifier characteristics for the ten MOSFET channels at a temperature of 10K, a V_{ss} of 15 volts, and a source load resistance (R_s) of 50 kilohms.

4.2 DEMONSTRATION OF ARRAY FUNCTIONALITY

After preamplifier characterization, MOSFET-gate load resistors were terminated to the ground traces on the MOSFET carrier substrates, which in turn were grounded to the metal package of the focal plane.

The focal plane was installed in a cryostat that included an indium antimonide LED for use as an infrared source. The LED had been characterized in earlier experiments, where it was found to emit a background of 6.67×10^{-9} W/cm^2 at a wavelength of 15 micrometers when operated with a current of 10 mA.

Row-output data were recorded with the room-temperature electronics connected and operated as described above (e.g., column bias sequentially switched). For recording, the S/H circuitry was connected to the input of a Spectral Dynamics SD360 spectrum analyzer operated in the "time domain" mode. The SD360 output was connected to a Hewlett-Packard HP 7035 X-Y recorder. The drive electronics was clocked, and output data were recorded per row for all 16 columns, with LED on and off, under the following conditions:

V_{read} = -10.13 volts
V_{store} = zero
t_{int} = integration time = 8 milliseconds
T = 10 K
H_{DC} = power flux at detector = 6.67×10^{-9} W/cm^2

TABLE 1 PREAMPLIFIER CHARACTERISTICS

FET No.	R_G (megohms)	C_{total} (pF)	Gain, G
1	35.0	2.0	0.82
2	30.8	2.4	0.82
3	30.5	2.35	0.83
4	32.4	2.18	0.81
5	31.5	2.23	0.80
6	31.2	1.73	0.60
7	31.3	2.11	0.63
8	30.5	2.01	0.69
9	29.6	2.48	0.78
10	28.8	2.50	0.81

Each row displayed a change in output signal due to illumination. Figure 15 shows typical row-output signals.

4.3 CURRENT RESPONSIVITY

Row 1 was chosen for the characterization of change in responsivity due to variations in V_{read} and V_{store}, temperature, and integration time. Current responsivity (R_I) was calculated from

$$R_I = \frac{SC_{total}}{H_{DC}\ A\ t_{int}\ G}$$

where

S = signal change, volts

C_{total} = total capacitance of MOSFET preamplifier, farads

H_{DC} = power flux at detector, W/cm^2

t_{int} = integration time, seconds

G = total system gain

A = detector area, cm^2

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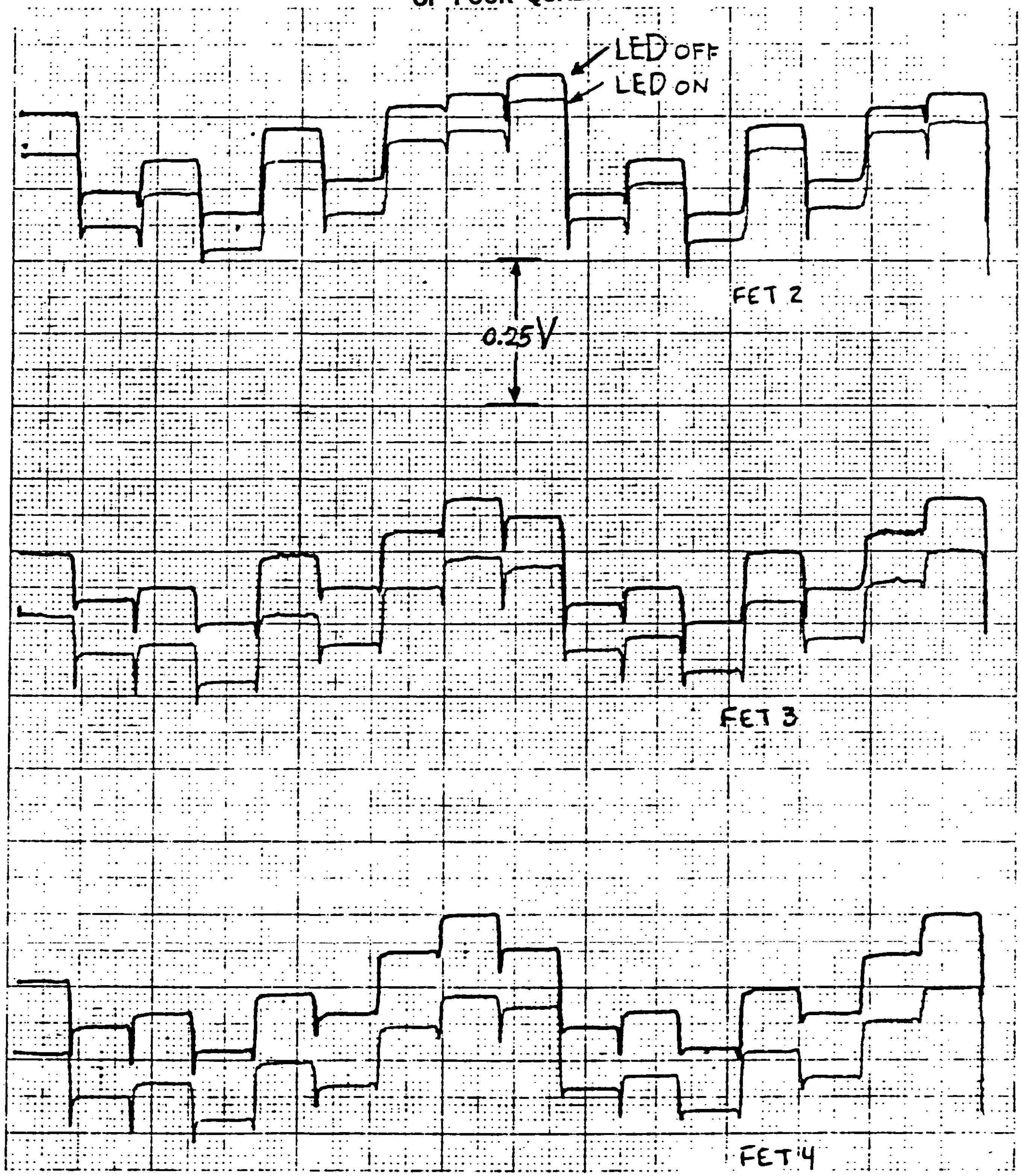


FIGURE 15 TYPICAL MOSAIC-ARRAY OUTPUT SIGNALS

The values for C_{total} and G were obtained from Table 1. The detector area was 64 mils^2. Responsivity change with V_{store} changes is shown in Table 2, with with integration time in Table 3, and with V_{read} changes (V_{store} constant) in Figures 16 and 17 (which represent columns 1 and 8, respectively).

Signal output vs temperature showed no significant change for either 12 K or 8 K, as compared with 10 K data. Hence, 10 K is suggested as a reasonable operating point.

Signal output increased with increased V_{store} up to 1 volt, but decreased at higher voltages. A more thorough optimization can be obtained by checking at finer potential increments between zero and 1 volt.

Responsivity vs integration time was nonuniform for array columns 9 through 16, and remained relatively constant for columns 1 through 8. This could occur if there is a difference in maximum well capacity for each column; columns 9 through 16 would then be in saturation at integration times exceeding 16 milliseconds.

Responsivity showed an increase as a function of V_{read}, which was expected.

All measurements were made with the guard grounded. Measurements on previous AMCIDs have shown that a small potential ($<\underline{+}1$ volt) on the guard reduces crosstalk between columns and tends to make the output signal more uniform columnwise.

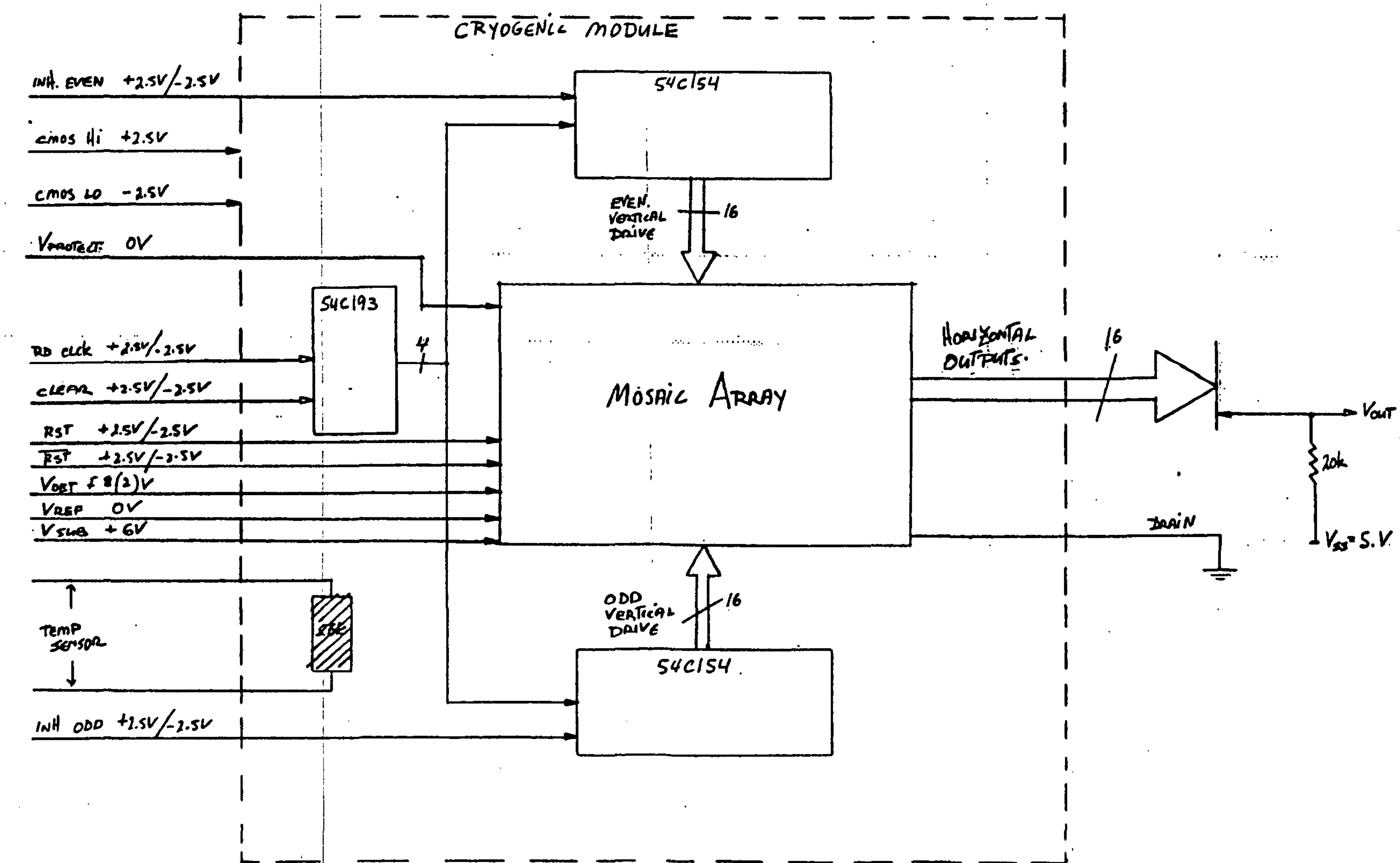
4.4 SPECTRAL RESPONSE

No spectral-response data were obtained for this device, but Figure 18 reproduces a spectral-response curve for an AMCID detector with similar depth and doping density.

Appendix C

The 16x32 MOS-FET Multiplexed Array

Figure 1. I/O BLOCK DIAGRAM FOR THE 16x32 MOSAIC MODULE



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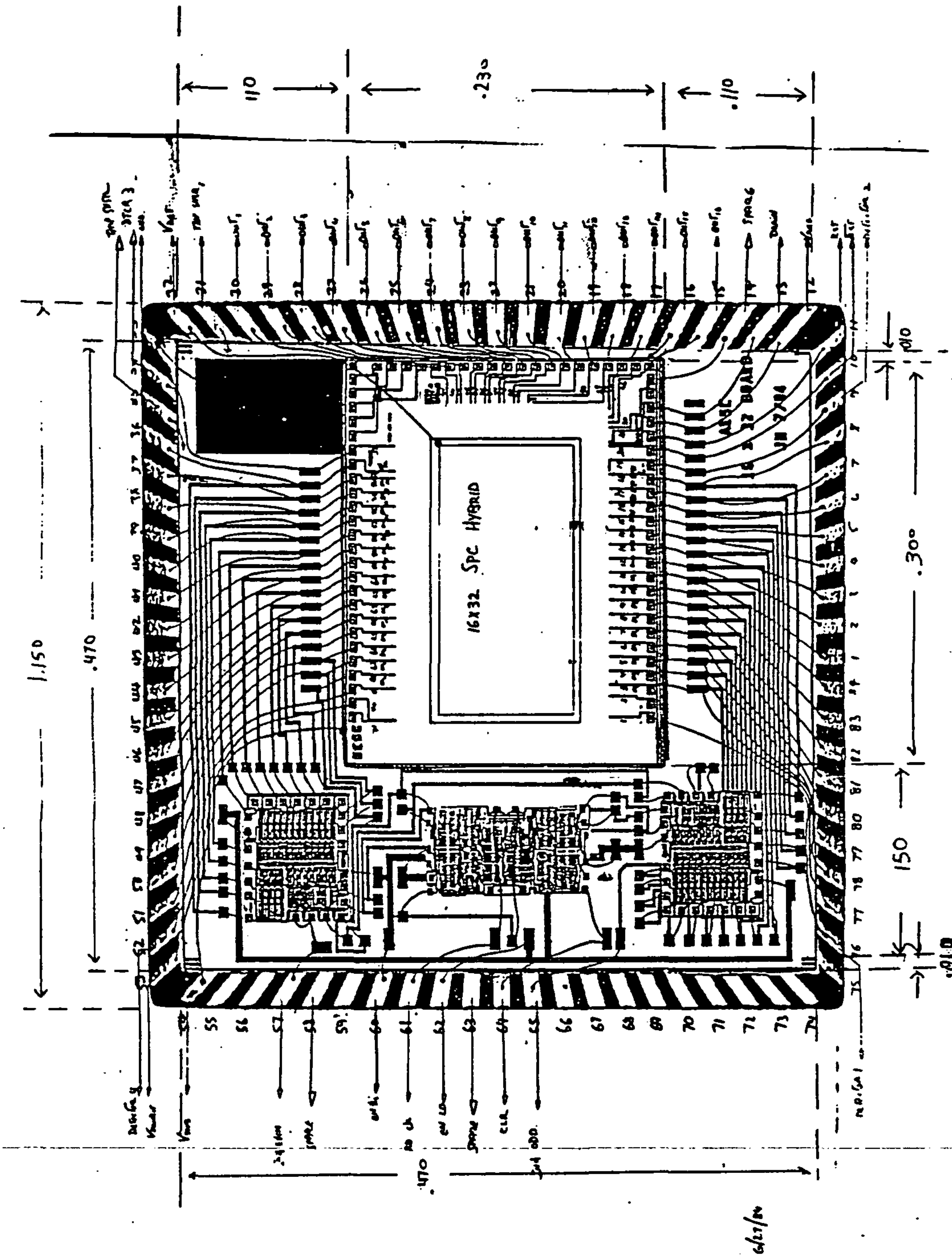

Figure 2. The 16 x 32 array layout.

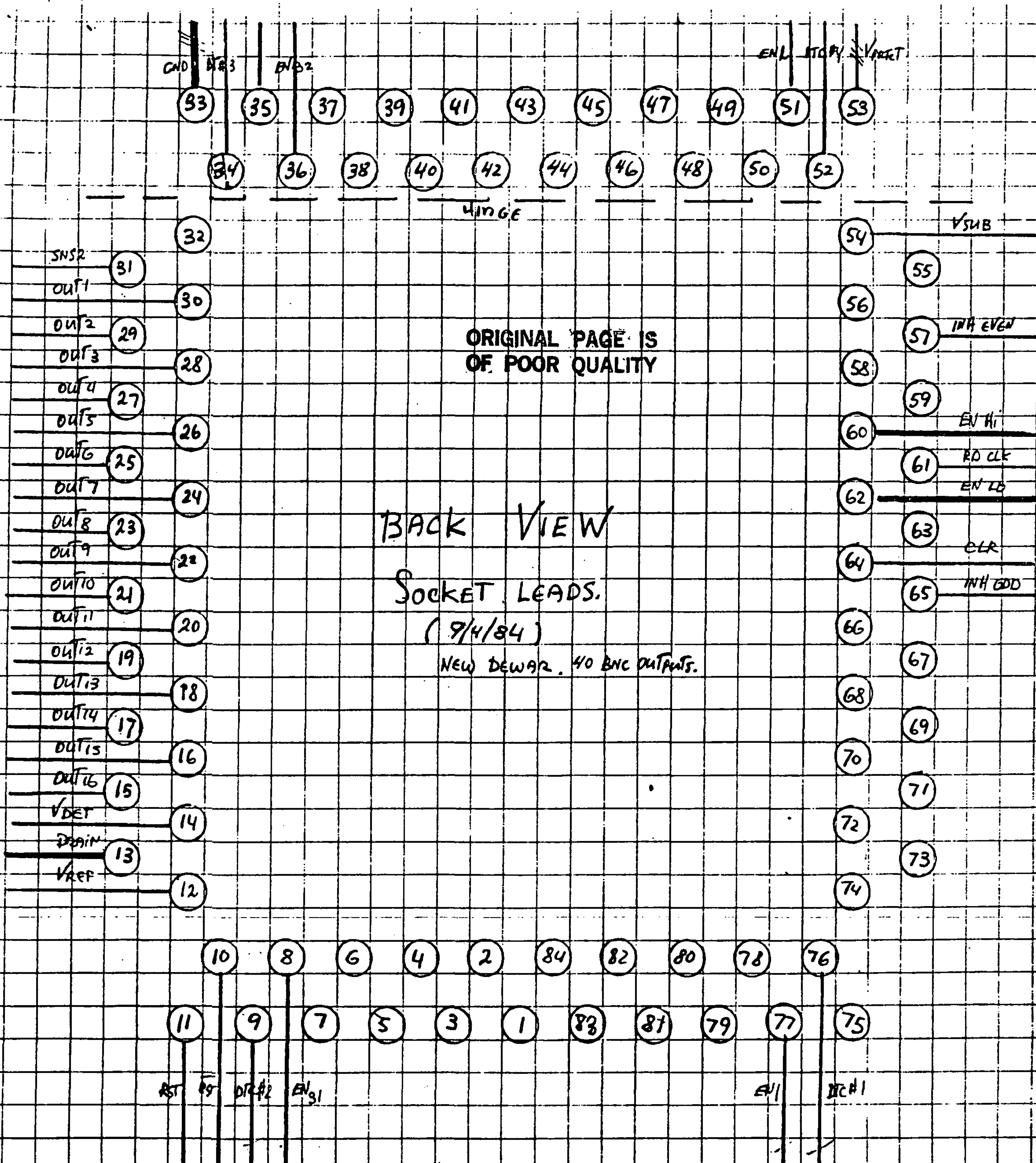

Figure 3. 16 x 32 array electrical connections.

Figure 4. HYBRID AND PREPROCESSOR CONTROLLER

REF DESIG	P/N
U1	4017B
U2	74C74
U3	40193B
U4,5	4585B
U7	4050B
U8,9,10	74C221
U11,12	74C00
U13	74C32
U6,14,17,19	4041UB
U15,16,18	HCPL 2200
R1-R12	10k, 5%, 1/8W.
R13-R17	20K 10Turns
R18-R20	1.1k, 5%, 1/8W
C1-C8,C17	.1μF, ceramic
C9-C11	120pF "
C12,C13,C16	400pF "
C14	1000pF "
C15	3000pF "

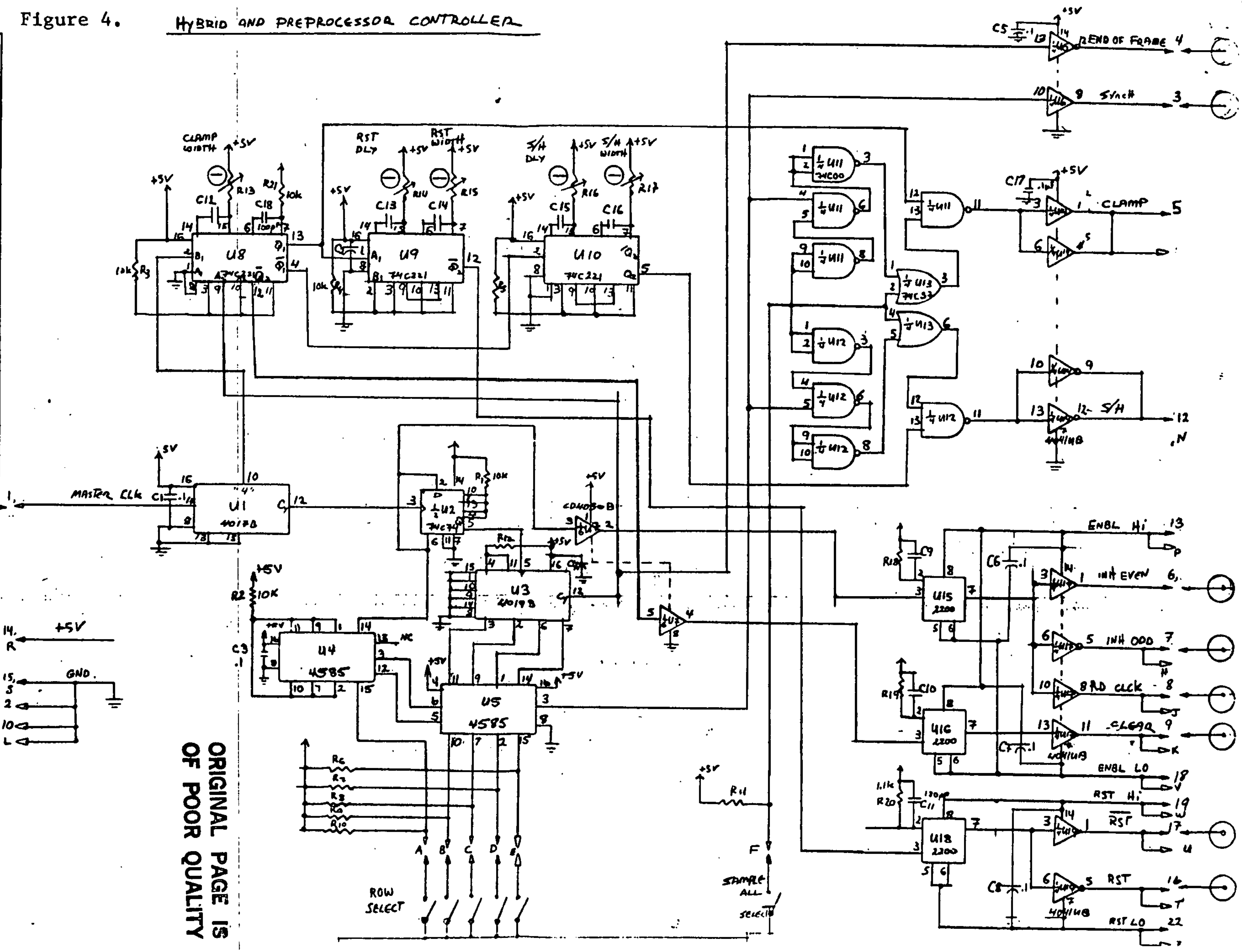

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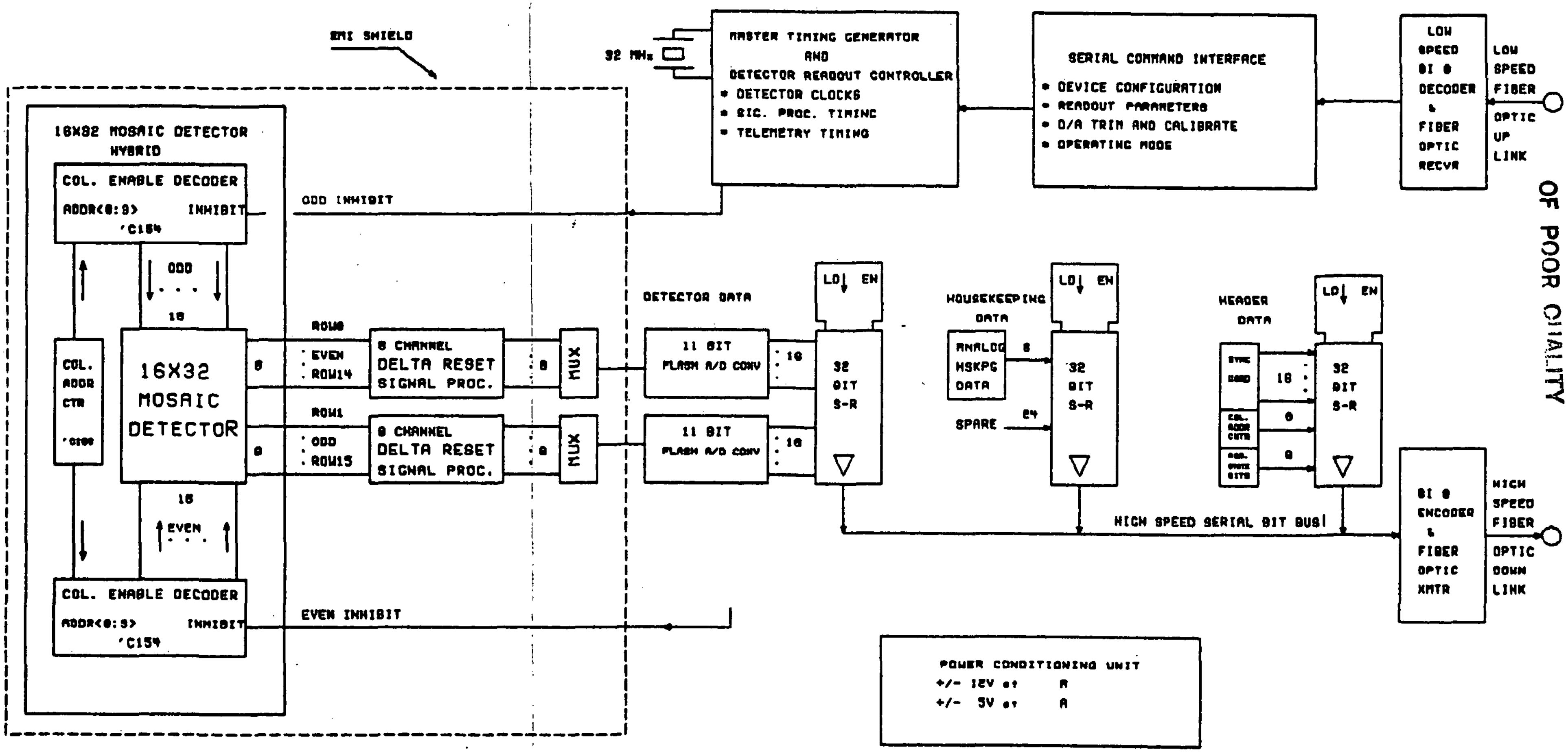
Figure 5. Block diagram of readout electronics.



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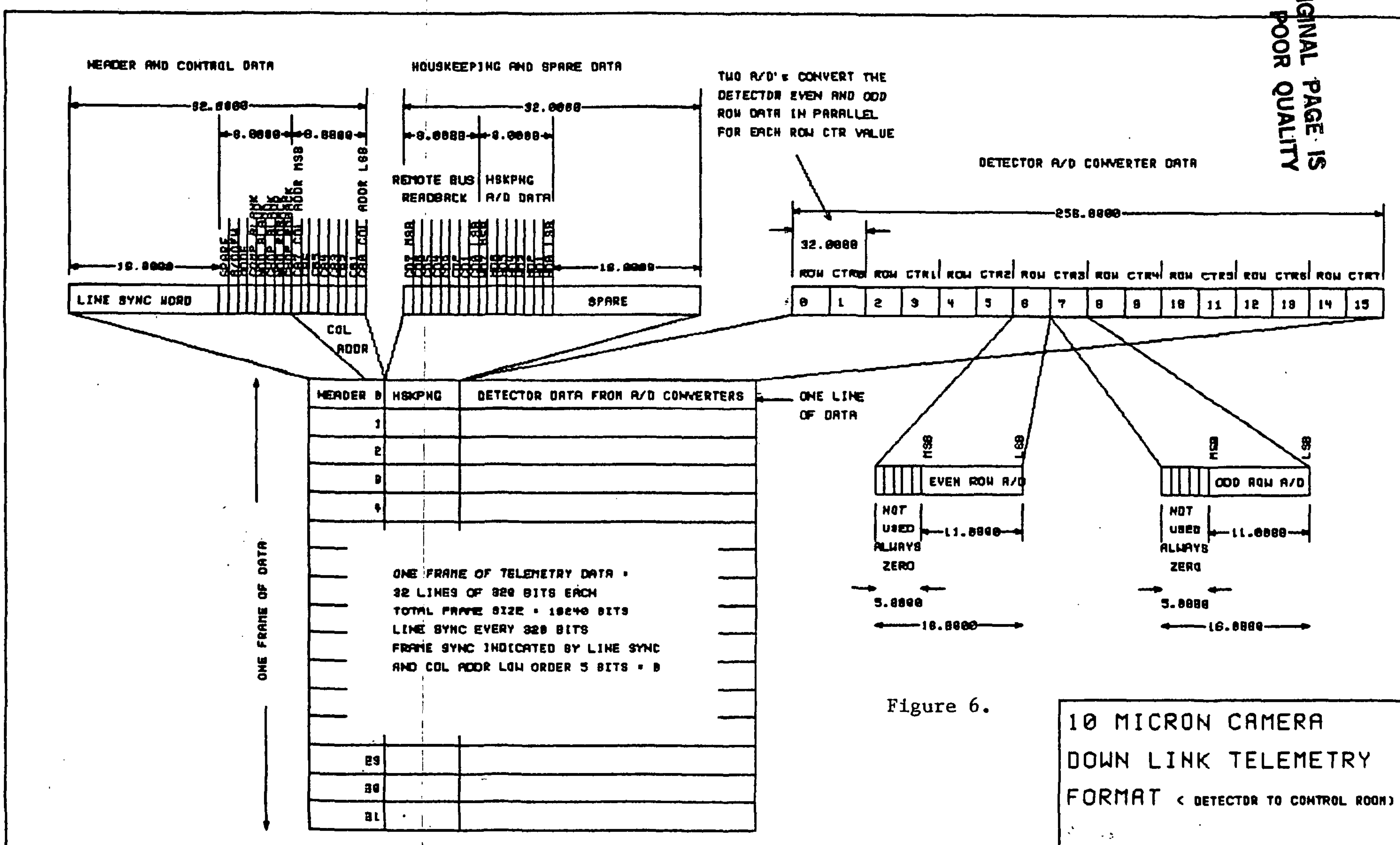

Figure 6.